IN THE CLAIMS:

1 (presently amended). A semiconductor device comprising:

a thyristor having thyristor body regions including first and second immediately adjacent base regions between first and second emitter regions;

a first control port configured and arranged to capacitively couple a first signal at least to the first base region; and

a second control port configured and arranged for receiving a second signal generated outside of the thyristor and for coupling [[a]] the second signal at least to the second base region, the second signal being adapted to control holding current or forward blocking voltage of the thyristor as a function of temperature.

2 (original). The semiconductor device of claim 1, further comprising:

a circuit arrangement electrically coupled to the second control port and configured and arranged to apply the second signal to the second control port.

3 (original). The semiconductor device of claim 2, wherein the circuit arrangement includes a temperature sensing circuit electrically coupled to the thyristor and configured and arranged to apply the second signal to the second control port as a function of the temperature of the thyristor.

4 (original). The semiconductor device of claim 2, wherein the second signal applied by the temperature sensing circuit is adapted to increase bipolar gains of the thyristor when the temperature of the thyristor is below a selected threshold.

5 (original). The semiconductor device of claim 4, wherein the selected threshold is a temperature at which the holding current of the thyristor would exceed a design holding current value.

6 (presently amended). A memory device comprising:

at least one thyristor having thyristor body regions including first and second immediately adjacent base regions respectively coupled to and between first and second emitter regions;

a first control port configured and arranged to capacitively couple a first signal at least to the first base region;

a first circuit configured and arranged to detect a temperature-related failure of the thyristor to maintain its conductance state during a standby mode or to maintain its blocking state; and

a second circuit including a second control port configured and arranged for receiving a second signal generated outside of the thyristor and for coupling [[a]] the second signal at least to the second base region as a function of the detected failure for controlling holding current or forward blocking voltage of the thyristor.

7 (original). The memory device of claim 6, further comprising a reference thyristor, the first circuit being configured and arranged to detect the failure condition from the reference thyristor.

8 (original). The memory device of claim 7, wherein the reference thyristor is configured and arranged to exhibit temperature-responsive failure prior to the at least one thyristor as the operating temperature of the memory device varies from a design operating temperature thereof.

9 (original). The memory device of claim 8, wherein the reference thyristor is configured and arranged to fail at a lower temperature than the at least one thyristor as the operating temperature increases above the design operating temperature.

10 (original). The memory device of claim 8, wherein the reference thyristor is configured and arranged to fail at a higher temperature than the at least one thyristor as the operating temperature decreases below the design operating temperature.

11 (original). The memory device of claim 6, further comprising a plurality of memory cells, each memory cell including a thyristor, wherein the first circuit further comprises:

a first reference memory cell including a thyristor and adapted to store a data "zero" and to fail to retain the data "zero" as a function of the conductance state of the thyristor in the first reference memory cell before other memory cells in the memory device fail data "zero";

a second reference memory cell including a thyristor and adapted to store a data "one" and to fail to retain the data "one" as a function of the conductance state of the thyristor in the second reference memory cell before other memory cells in the memory device fail data "one"; and

the second circuit being adapted to apply the second signal to the second control port as a function of at least one of the first and second reference memory cells failing to retain data.

12 (original). The memory device of claim 11, wherein an emitter of the thyristor in the first reference memory cell is coupled to a reference voltage signal that is greater than a reference voltage signal coupled to at least one of the emitter regions of the thyristors in the plurality of memory cells.

13 (original). The memory device of claim 11, wherein an emitter of the thyristor in the first reference memory cell is coupled to a reference voltage signal that is less than a reference voltage signal coupled to at least one of the emitter regions of the thyristors in the plurality of memory cells.

14 (original). The memory device of claim 11, wherein each memory cell includes a pass device coupled to an emitter region of the respective thyristor, each pass device exhibiting leakage, the pass device in the second reference thyristor memory cell being adapted to leak relatively more current than the pass devices in the plurality of memory cells such that the second reference memory cell fails to retain data before the plurality of memory cells fail to retain data.

15 (presently amended). The memory device of claim 6, wherein the second control port and the second base region are configured and arranged such that the second signal increases carrier depletion in the second base region ~~in the second base region~~.

16 (original). The memory device of claim 6, wherein the second control port extends over a junction between the second base region and the second emitter region.

17 (original). The memory device of claim 16, wherein the second circuit is adapted to capacitively couple the second signal to the second emitter region for accumulating carriers therein.

18 (original). The memory device of claim 6, wherein the second control port extends over a junction between the first and second base regions.

19 (presently amended). A semiconductor device comprising:

a thyristor having thyristor body regions including first and second immediately adjacent base regions between first and second emitter regions, the thyristor body being maintained in a conductance state as a function of holding current; and

a control circuit configured and arranged for applying a signal to at least one of the base regions for controlling the holding current or forward blocking voltage as a function of temperature, the signal being generated outside of the thyristor.

20 (original). The semiconductor device of claim 19, wherein the thyristor is a thin capacitively-coupled thyristor.

21 (original). The memory device of claim 6, wherein the thyristor is a thin capacitively-coupled thyristor.

22 (presently amended). The ~~memory~~ semiconductor device of claim 1, wherein the thyristor is a thin capacitively-coupled thyristor.

23 (presently amended). The ~~memory~~ semiconductor device of claim 1, wherein one of the base regions includes N-doped material having a higher concentration of N+ dopant in a depletion region that faces the second control port.

24 (presently amended). The ~~memory~~ semiconductor device of claim 1, wherein one of the base regions includes material having defects in a depletion region facing the second control port.

25 (original). The memory device of claim 6, wherein one of the base regions includes N-doped material having a higher concentration of N+ dopant in a depletion region that faces the second control port.

26 (original). The memory device of claim 6, wherein one of the base regions includes material having defects in a depletion region facing the second control port.

27 (original). The semiconductor device of claim 19 further comprising a second control port, wherein one of the base regions includes N-doped material having a higher concentration of N+ dopant in a depletion region that faces the second control port.

28. (cancelled)